



**REPLY UNDER 37 C.F.R. § 1.116  
EXPEDITED PROCEDURE  
EXAMINING GROUP 2133**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Application No.: 10/037,361  
Filed: October 29, 2001  
Inventor:  
James M. Byrd

Examiner: Gandhi, Dipakkumar B.  
Group/Art Unit: 2133  
Atty. Dkt. No: 5181-94400

Title: System and Method for  
Verifying Error  
Detection/Correction Logic

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

Robert C. Kowert

Printed Name

[Signature] May 23,  
Signature Date

May 23, 2005

Date \_\_\_\_\_

**RESPONSE TO OFFICE ACTION OF  
MARCH 21, 2005**

**Mail Stop AF**  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

This paper is submitted in response to the Final Action of March 21, 2005, to further highlight why the application is in condition for allowance.

Please amend the case as listed below.